# Higher Logic

	5510					
NOT Gate						
	The output Z is the opposite of the input A. If the input is 0 (low) then the output will be 1 (high).		D :	<b>z</b> 1 0	Boolean expression Ā = Z	NAND Equivalent
AND Gate		Α	В	z		
	The output Z will only be high (1)	0	0	0	Boolean expression	NAND Equivalent
	when both input A and B are	0	1	0	A . B = Z	
	high (1).	1	0	0		
AND		1	1	1		
OR Gate		Α	В	z		
		0	0	0	Boolean expression	NAND Equivalent
$ \rightarrow $	The output Z will be high (1) when either input A or B or both	0	1	1	A + B = Z	
7	inputs are high (1).	1	0	1		
OR		1	1	1		
		<b></b>	1	1	1	
NAND	The NAND is the opposite of the	Α	В	Z	Declary oversign	
	AND. The output Z will only be	0	0	1	Boolean expression	
	low (0) when both input A and B	0	1	1	$\overline{A \cdot B} = Z$	
NAND	are high (1).	1	1	0		
			_	Ĵ		
NOR Gate		Α	В	z		
	The NOR is the opposite of the	0	0	1	Boolean expression	NAND Equivalent
$\square \rightarrow$	OR. The output Z will only be	0	1	0	$\overline{A + B} = Z$	
	high (1) when input A and B are	1	0	0	-	
NOR	low (0).	1	1	0		
XOR Gate		Α	В	z		
		0	0	0	Boolean expression	NAND Equivalent
$(\neg)$	The output Z will only be high (1)	0	1	1	A⊕B = Z	+
	when only one input is high (1).	1	0	1		
XOR		1	1	0	]	
1						

### **Developing Boolean expressions from circuits** A + B Α (A + B) . B В $(A + B) \cdot B = Z$ В **Developing Boolean expressions from truth tables** В С Ζ Α is high (1). 0 0 0 0 2 - Create an expression for that row. 0 0 1 Ā.B.C 1 0 0 0 1 using the OR expression in between. Ā.B.C 0 1 1 1 0 0 1 0 1 0 1 1 A.B.C 0 1 0 1 1 1 1

## **Developing Boolean expressions from word problems**

Input/Output	Operation
alarm sounds	Z=1
gates open	A=0
maximum loading exceeded	B=1
button C pressed	C=1
button D pressed	D=1

A proposed design has the following specification (all conditions must be met). The alarm (Z):

• will not sound unless the gate (A) is closed From the table A = 1

1

A.B.C

- will not sound when the weight on the platform exceeds the maximum loading (B) From the table B = 0
- will sound when either button (C) or (D) is pressed, but not when both are pressed at the same time.  $C \oplus D$
- (a) Complete the Boolean equation for the alarm system in operation.

 $Z = A \cdot \overline{B} \cdot (C + D)$ 

1 - Look for the rows of the truth table where output Z

3 - Create an overall expression for all of the rows

 $Z = (\overline{A} \cdot \overline{B} \cdot C) + (\overline{A} \cdot B \cdot C) + (A \cdot \overline{B} \cdot C) + (A \cdot B \cdot C)$ 

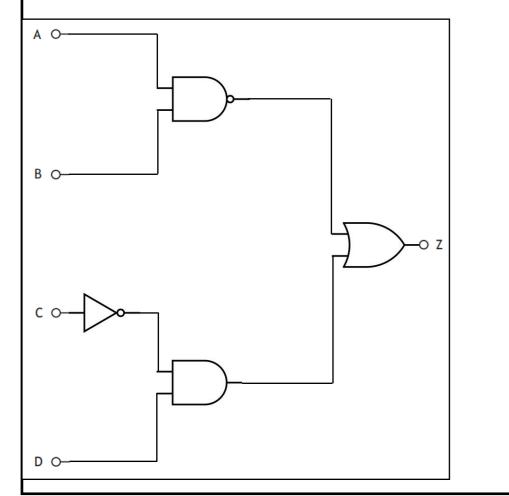
Start by figuring out what each of the inputs need to be doing for the alarm to sound. If it must happen then there needs to be . between the inputs in the expression.

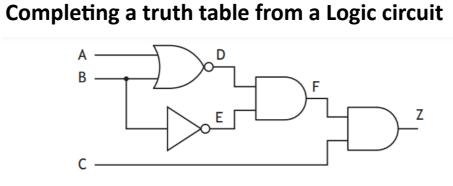
### Developing a circuit from a Boolean expression

 $Z = (\overline{A \cdot B}) + (\overline{C} \cdot D)$ 

1 - Start by figuring out how many logic gates you will need and what type they are.

- In this example there are 4 inputs.
- 2 inputs are going into a NAND gate and the other 2 inputs into an AND gate. We know this from the . between the expressions in the brackets.
- The output from those gates are going into an OR gate. We know this from the + in between the 2 expressions.
- C is inverted so there needs to be a NOT gate too.





To complete this type of question you will need to have a sound knowledge of the different logic gates and their truth tables.

Column D is d gate.

Complete the truth table for the logic diagram.

Include the intermediate logic values for D, E and F.

Α	В	С	D	E	F	Z	
0	0	0					
0	0	1					
0	1	0					
0	1	1					Column E is
1	0	0					Column F is
1	0	1					gate.
1	1	0					Column Z is
1	1	1					
	0 0 0	0         0           0         0           0         1           0         1           1         0	0         0         0           0         0         1           0         1         0           0         1         1           1         0         0           1         0         1	0         0         0         0           0         0         1         1           0         1         1         1           1         0         0         1           1         0         1         1	0       0       0       0         0       0       1	0       0       0       0       0         0       0       1       0       0         0       1       0       0       0         0       1       1       0       0         1       0       0       1       0         1       0       1       0       0	0       1       0       0       0       1       0       0       1       1       0       0       1       1       0       0       1       1       0       0       1       1       0       0       1       1       0       1       1       0       1       1       0       1       1       0       1       1       0       1       1       0       1       1       0       1       1       0       1

		D	E	F	Z
) (	D	1	1	1	0
)	1	1	1	1	1
(	0	0	0	0	0
	1	0	0	0	0
) (	0	0	1	0	0
) '	1	0	1	0	0
(	0	0	0	0	0
	1	0	0	0	0
		) 1 I 0 I 1 ) 0	$\begin{array}{c ccccc} & - & - & - \\ \hline 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 1 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \\ \end{array}$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$

NAND Equivalent advantages

Fewer IC chips required to make circuits meaning a simpler construction.

Fewer ICs meaning smaller product size.

Fewer ICs means reduced cost.

Buying NAND gates in bulk would lower the cost rather than buying different types of gates to perform the same function.

Column D is dependant on A and B going through a NOR

Α	В	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

s the opposite of B.

s dependant on D and E going through an AND

s dependant on F and C.

Α	В	AND
0	0	0
0	1	0
1	0	0
1	1	1